

NORTH SOUTH UNIVERSITY

Department of Electrical & Computer Engineering

**Fall 2018**

**Course ID: CSE332**

Course Title: Computer Organization and Architecture

Project: Instruction Set Architecture (ISA)

Section: 1

Group No: 6

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|  |  |
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**Introduction:**

Our task was to design 10 bit single-cycle (RISC) CPU that has separate Data and Instruction Memory.

**Objective:**

We have to design our ISA focusing on the following three categories of programs:

a) Simple arithmetic & logic operations

b) Programs that require checking conditions

c) Loop type of programs

**Operands:**

We’ve used 0-2 (depends on ISA format) operands in our ISA. Most of them are register based and some are constant.

We’ve used 4 registers and assigned 2 bits for the saved registers, 1 bit for a zero register and another bit for a temporary register. The Register we have selected are given below:

|  |  |
| --- | --- |
| Name | Value Assigned |
| $zero | 000 |
| $s0 | 001 |
| $s1 | 010 |
| $s2 | 011 |
| $t0 | 100 |
| $t1 | 101 |
| $t2 | 110 |
| $acc | 111 |

**Operations:**

There are 16 different operations. Syntax Rules:

1. There must be at least a single **space** between the opcode and the trailing contents.
2. If there are multiple operands, there must a **comma** after the first operand.
3. System allocated register name always starts with the **‘$’** -sign.
4. Constant starts with the **‘#’** – sign.
5. There can not be any space after the register and constant signs.
6. The instructions are **not case-sensitive**.

The details are given below:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Category** | **Operation** | **Syntax** | **Meaning** | **Comments** |
| Arithmetic | add | add $s1, $s2 | $acc = $s1 + $s2 | Two register operands |
| subtract | sub $s1, $s2 | $acc = $s1 - $s2 | Two register operands |
| add immediate | addi $s1, #const | $acc = $s1 + constant | Used to add constants |
| Data Transfer | load accumulator | lda #const | $acc = Memory[constant] | Loads from memory to accumulator |
| store accumulator | sta #const | Memory[constant] = $acc | Stores into memory from accumulator |
| Move register value | mov $s1, $s2 | $s1 = $s2 | Moves the value of reg2 to reg1 |
| Move immediate value | movi $s1, #const | $s1 = constant | Moves the constant into reg2 |
| Logical | AND | and $s1, $s2 | $acc = $s1 & $s2 | And operation |
| OR | or $s1, $s2 | $acc = $s1 | $s2 | Or operation |
| NOR | nor $s1, $s2 | $acc = ~($d | $s) | Nor operation |
| Conditional  branch | Jump if equal | jeq $s1, #target | If ($acc == $s1)  Jump to Target | If the register value is equal to the accumulator then jump to target |
| Jump if not equal | jne $s1, #target | If ($acc != $s1)  Jump to Target | If the register value is not equal to the accumulator then jump to target |
| Jump if less than | jlt $s1, #target | If ($acc < $s1)  Jump to Target | If the register value is less than the accumulator then jump to target |
| Unconditional  Jump | Jump | jmp #target | Jump to target address | After checking conditions, use jmp to break loop. |
| External Communication | In | in #const | $acc = from a port with the provided address | Perform input operations |
| Out | out #const | to a port with the provided address = $acc | Perform output operations |

**Format:**

The format and op code for 3 different ISA type are given below:

**RA-Type List:**

6 operations. Used for register-register arithmetic operations and moving.

|  |  |
| --- | --- |
| Operation | Op-code |
| add | 0000 |
| sub | 0001 |
| and | 0010 |
| or | 0011 |
| nor | 0100 |
| mov | 0101 |

**RA-Type ISA format:**

|  |  |  |
| --- | --- | --- |
| Op-code | rs | rt |
| Bits: 4 bits | 3 bits | 3 bits |

**IB-Type List:**

5 operations. Used for immediate operations and Branching.

|  |  |
| --- | --- |
| Operation | Op code |
| addi | 0110 |
| movi | 0111 |
| jeq | 1000 |
| Jne | 1001 |
| jlt | 1010 |

**IM-Type ISA format:**

|  |  |  |
| --- | --- | --- |
| Op code | rs | Immediate |
| Bits: 4 bits | 3 bits | 3 bits |

**JC-TYPE LIST:**

5 operations. Used for Jump and Call.

|  |  |
| --- | --- |
| Operation | Op code |
| lda | 1011 |
| sta | 1100 |
| in | 1101 |
| out | 1110 |
| jmp | 1111 |

**JC-Type ISA format:**

|  |  |
| --- | --- |
| Op-code | Target |
| Bits: 4 bits | 6 bits |